

# KA2S0965/KA2S09655

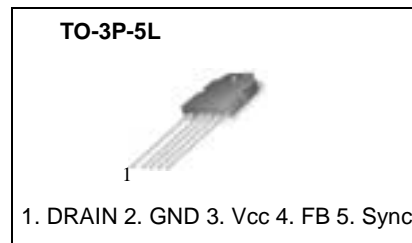
## Fairchild Power Switch(FPS)

### Features

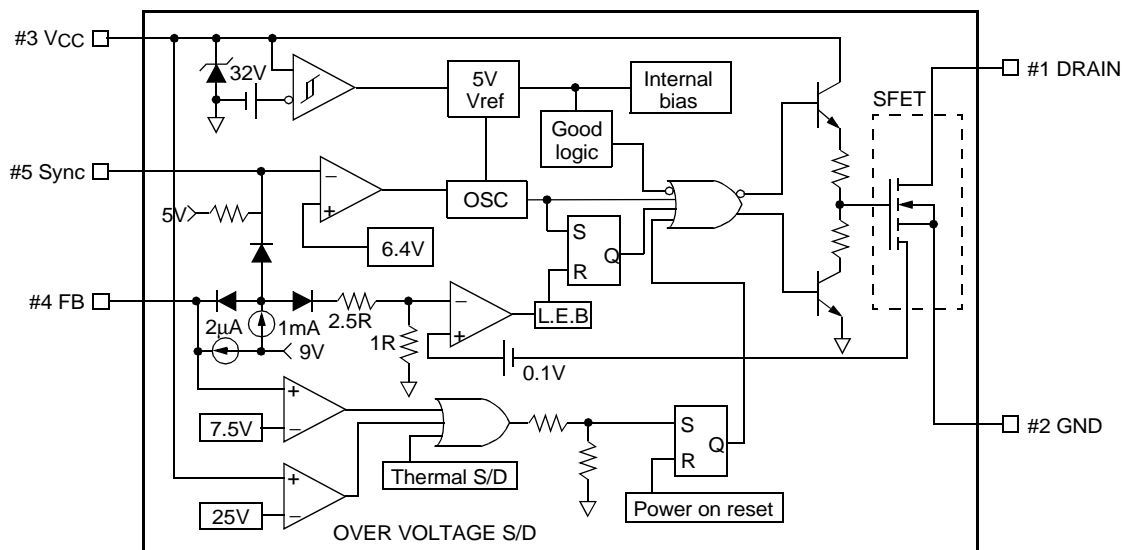
- Wide operating frequency range up to (150kHz)
- Pulse by pulse over current limiting
- Over load protection
- Over voltage protecton (Min. 23V)
- Internal thermal shutdown function
- Under voltage lockout
- Internal high voltage sense FET
- External sync terminal
- Latch up Mode

### Description

The Fairchild Power Switch(FPS) product family is specially designed for an off line SMPS with minimal external components. The Fairchild Power Switch(FPS) consist of high voltage power SenseFET and current mode PWM controller IC. control IC features a trimmed oscillator, under voltage lock out, leading edge blanking, optimized gate turn-on/turn-off driver, thermal shut down protection, over voltage protection, temperature compensated precision current sources for loop compensation and fault protection circuit. compared to discrete MOSFET and controller or RCC switching converter solution, a Fairchild Power Switch(FPS) can reduce total component count, design size, weight and at the same time increase & efficiency, productivity, and system reliability. It has a basic platform well suited for cost effective Monitor power supply.



### Internal Block Diagram



## Absolute Maximum Ratings

Characteristic	Symbol	Value	Unit
Maximum Drain voltage <sup>(1)</sup>	V <sub>D,MAX</sub>	650	V
Drain Gate voltage (R <sub>GS</sub> =1MΩ)	V <sub>DGR</sub>	650	V
Gate source (GND) voltage	V <sub>GS</sub>	±30	V
Drain current pulsed <sup>(2)</sup>	I <sub>DM</sub>	36.0	ADC
Single pulsed avalanche energy <sup>(3)</sup>	E <sub>AS</sub>	950	mJ
Continuous drain current (T <sub>C</sub> =25°C)	I <sub>D</sub>	9.0	ADC
Continuous drain current (T <sub>C</sub> =100°C)	I <sub>D</sub>	5.8	ADC
Maximum Supply voltage	V <sub>CC,MAX</sub>	30	V
Input voltage range	V <sub>FB</sub>	-0.3 to V <sub>SD</sub>	V
Total power dissipation	P <sub>D</sub>	170	W
	Derating	1.33	W/°C
Operating ambient temperature	T <sub>A</sub>	-25 to +85	°C
Storage temperature	T <sub>STG</sub>	-55 to +150	°C

**Note:**

1. T<sub>j</sub>=25°C to 150°
2. Repetitive rating: Pulse width limited by maximum junction temperature
3. L=20mH, V<sub>DD</sub>=50V, R<sub>G</sub>=27Ω, starting T<sub>j</sub>=25 °C

## Electrical Characteristics (SFET part)

(Ta = 25°C unless otherwise specified)

Characteristic	Symbol	Test condition	Min.	Typ.	Max.	Unit
Drain source breakdown voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =50μA	650	-	-	V
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> =Max., Rating, V <sub>GS</sub> =0V	-	-	50	μA
		V <sub>DS</sub> =0.8Max., Rating, V <sub>GS</sub> =0V, T <sub>C</sub> =125°C	-	-	200	mA
Static drain source on resistance <sup>(note)</sup>	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =4.5A	-	0.96	1.2	W
Forward transconductance <sup>(note)</sup>	g <sub>fs</sub>	V <sub>DS</sub> =50V, I <sub>D</sub> =4.5A	5.0	-	-	S
Input capacitance	C <sub>iss</sub>	V <sub>GS</sub> =0V, V <sub>DS</sub> =25V, f=1MHz	-	1750	-	pF
Output capacitance	C <sub>oss</sub>		-	190	-	
Reverse transfer capacitance	C <sub>rss</sub>		-	78	-	
Turn on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> =0.5BV <sub>DSS</sub> , I <sub>D</sub> =9.0A (MOSFET switching time are essentially independent of operating temperature)	-	20	50	nS
Rise time	t <sub>r</sub>		-	23	55	
Turn off delay time	t <sub>d(off)</sub>		-	85	180	
Fall time	t <sub>f</sub>		-	30	70	
Total gate charge (gate-source+gate-drain)	Q <sub>g</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =9.0A, V <sub>DS</sub> =0.5BV <sub>DSS</sub> (MOSFET switching time are essentially independent of operating temperature)	-	74	95	nC
Gate source charge	Q <sub>gs</sub>		-	12	-	
Gate drain (Miller) charge	Q <sub>gd</sub>		-	35.4	-	

**Note:**

Pulse test: Pulse width ≤ 300μS, duty cycle ≤ 2%

$$S = \frac{1}{R}$$

## Electrical Characteristics (CONTROL part)

(Ta = 25°C unless otherwise specified)

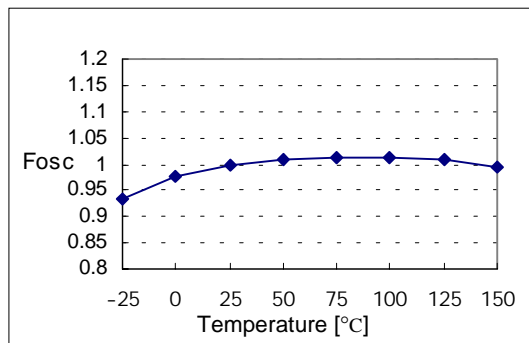
Characteristic	Symbol	Test condition	Min.	Typ.	Max.	Unit
<b>UVLO SECTION</b>						
Start threshold voltage	VSTART	-	14	15	16	V
Stop threshold voltage	VSTOP	After turn on	9	10	11	V
<b>OSCILLATOR SECTION</b>						
Initial accuracy	FOSC	Ta = 25°C	18	20	22	kHz
Frequency change with temperature <sup>(2)</sup>	$\Delta F/\Delta T$	-25°C ≤ Ta ≤ +85°C	-	±5	±10	%
Maximum duty cycle	DMAX	-	92	95	98	%
<b>FEEDBACK SECTION</b>						
Feedback source current	IFB	Ta = 25°C, Vfb = GND	0.8	1	1.2	mA
Shutdown Feedback voltage	VSD	-	6.9	7.5	8.1	V
Shutdown delay current	I <sub>delay</sub>	Ta=25°C, 5V ≤ Vfb ≤ VSD	1.4	1.8	2.2	μA
<b>SYNC. &amp; SOFT START SECTION</b>						
Soft start voltage	VSS	VFB = 2V	4.7	5.0	5.3	V
Soft start current	ISS	Sync & S/S = GND	0.8	-	-	mA
Sync threshold voltage <sup>(3)</sup>	VS <sub>YTH</sub>	Vfb = 5V	6.0	6.4	6.8	V
<b>REFERENCE SECTION</b>						
Output voltage <sup>(1)</sup>	Vref	Ta = 25°C	4.80	5.00	5.20	V
<b>PROTECTION SECTION</b>						
Thermal shutdown temperature (Tj) <sup>(1)</sup>	TSD	-	140	160	-	°C
Peak Current Limit	I <sub>OVER</sub>	KA2S0965	5.28	6.00	6.72	A
		KA2S09655	4.40	5.00	5.60	
<b>TOTAL DEVICE SECTION</b>						
Start Up current	I <sub>START</sub>	VCC = 14V	0.1	0.3	0.55	mA
Operating supply current (control part only)	I <sub>OP</sub>	Ta = 25°C	6	12	18	mA
VCC zener voltage	VZ	ICC = 20mA	30	32.5	35	V

### Note:

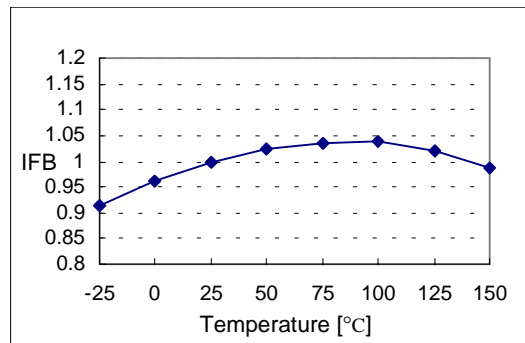
1. These parameters, although guaranteed, are not 100% tested in production
2. These parameters, although guaranteed, are tested in EDS(water test) process
3. The amplitude of the sync, pulse is recommended to be between 2V and 3V for stable sync function.

## Typical Performance Characteristics

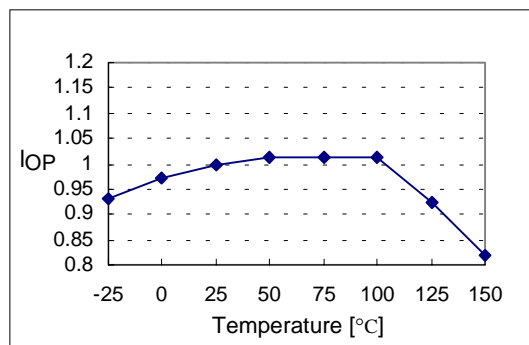
(These characteristic graphs are normalized at  $T_a = 25^\circ\text{C}$ )



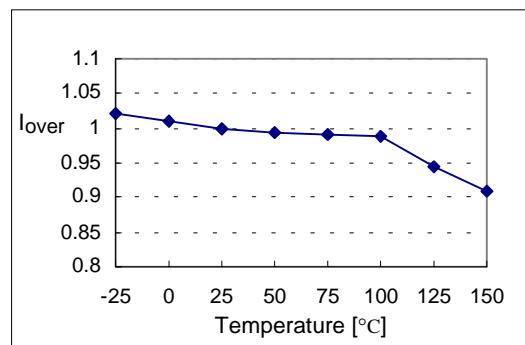
**Figure 1. Operating Frequency**



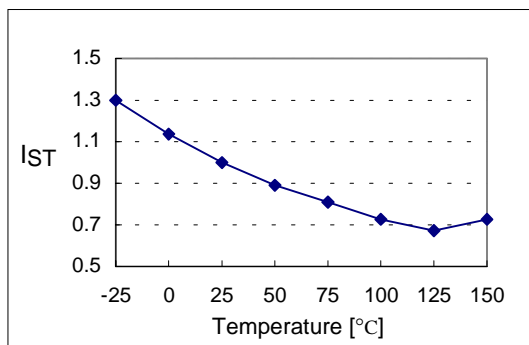
**Figure 2. Feedback Source Current**



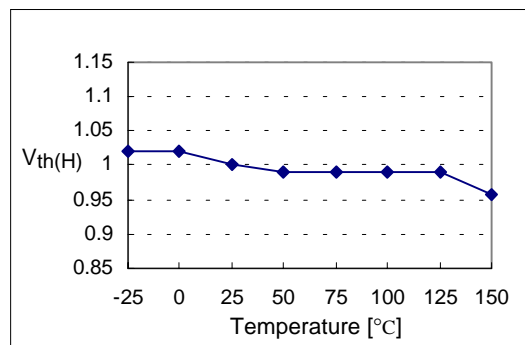
**Figure 3. Operating Supply Current**



**Figure 4. Peak Current Limit**



**Figure 5. Start up Current**



**Figure 6. Start Threshold Voltage**

## Typical Performance Characteristics (Continued)

(These characteristic graphs are normalized at  $T_a = 25^\circ\text{C}$ )



Figure 7. Stop Threshold Voltage



Figure 8. Maximum Duty Cycle



Figure 9. VCC Zener Voltage



Figure 10. Shutdown Feedback Voltage



Figure 11. Shutdown Delay Current



Figure 12. Over Voltage Protection

## Typical Performance Characteristics (Continued)

(These characteristic graphs are normalized at  $T_a = 25^\circ\text{C}$ )

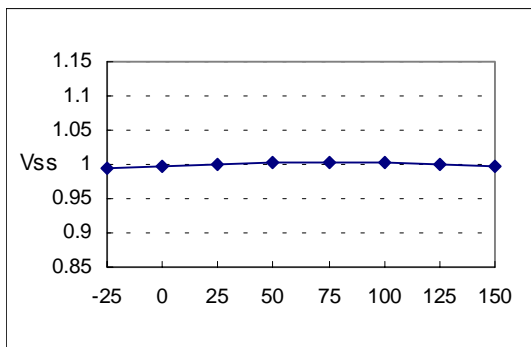


Figure13. Soft Start Voltage

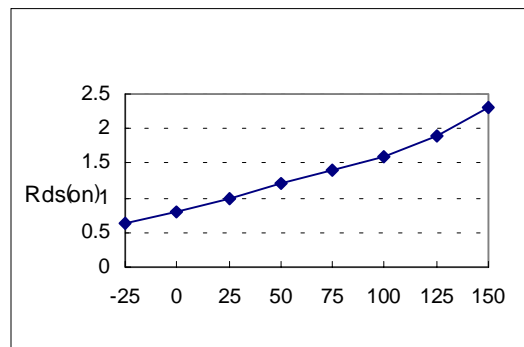
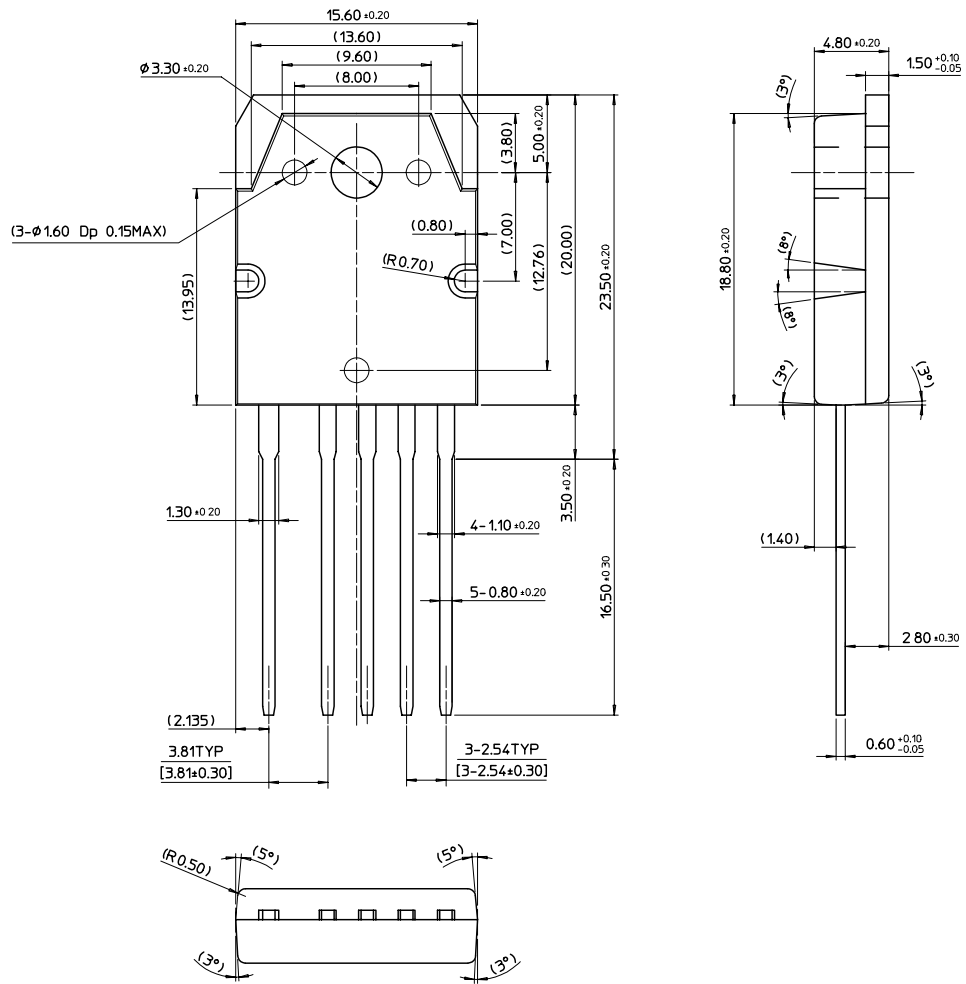


Figure 14. Static Drain-Source on Resistance

# Package Dimensions

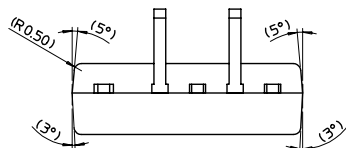
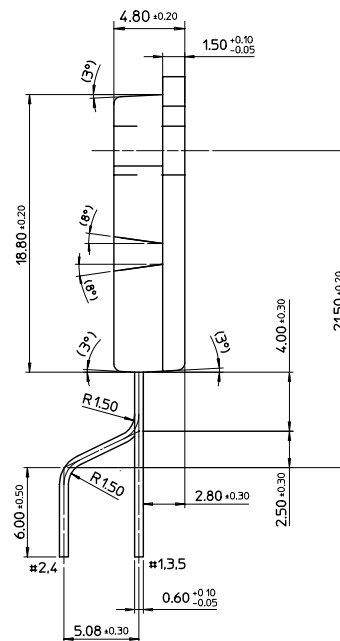
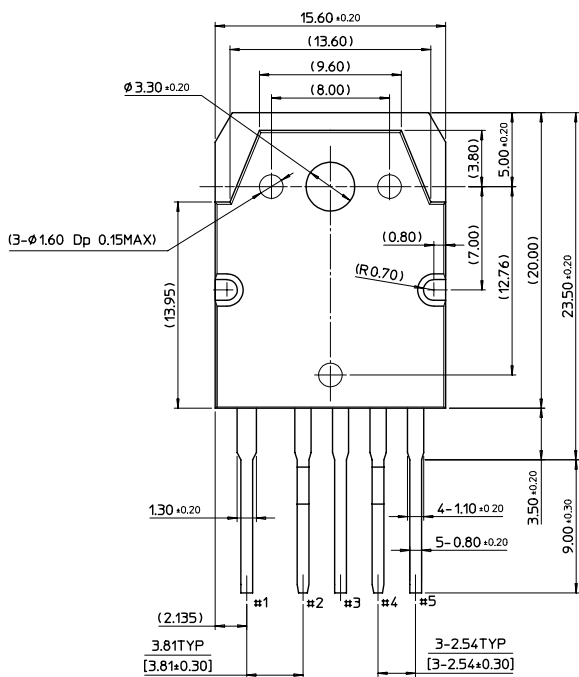
## TO-3P-5L





Package Dimensions (Continued)

TO-3P-5L (Forming)



## Ordering Information

Product Number	Package	Rating	Over current protection
KA2S0965-TU	TO-3P-5L	650V, 9A	6A
KA2S0965-YDTU	TO-3P-5L(Forming)		
KA2S09655-TU	TO-3P-5L	650V, 9A	5A
KA2S09655-YDTU	TO-3P-5L(Forming)		

TU : Non Forming Type

YDTU : Forming Type

### DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

### LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.